CLAIMS

What is claimed is:

1. A quadrature clock generating apparatus comprising:

a multiplexer selecting one of a generated clock and a gated generated clock as a double clock in accordance with a halt multiplexer control, wherein the double clock has a frequency twice that of a reference clock;

divider circuitry coupled to provide an alignment signal corresponding to an inverted double clock divided by two;

a recovery circuit for recovering a first clock and a second clock from the double clock in accordance with the alignment signal, wherein the first and second clocks have substantially a 90° phase difference; and

a halt circuit controlling the halt multiplexer control to select the gated generated clock when the alignment signal matches a pre-determined clock level, wherein the halt multiplexer control is clocked by the generated clock.

2. The apparatus of claim 1 wherein the recovery circuit comprises:

a first flip-flop receiving the alignment signal, wherein the first flip-flop is clocked by the double clock to provide the first clock; and

a second flip-flop receiving the first clock, wherein the second flip-flop is clocked by an inverted double clock to provide the second clock.

3. The apparatus of claim 2 wherein each of the first and second flip-flops is a D-type flip-flop.

4. The apparatus of claim 1 further comprising a phase locked loop to provide the generated clock.

5. The apparatus of claim 1 wherein the divider circuitry further comprises:

an inverter coupled to provide an inverted double clock; and

a divider coupled to divide the inverted double clock to provide the alignment signal.

6. The apparatus of claim 1 wherein the clock generator, divider, and recovery circuitry reside on a same integrated circuit die.

7. The apparatus of claim 6 wherein the clock generator, divider and recovery circuitry are formed as a metal oxide semiconductor field effect transistor (MOSFET) integrated circuit.

8. A quadrature clock generation apparatus, comprising:

a multiplexer selecting one of a generated clock and a gated generated clock as a double clock in accordance with a halt multiplexer control, wherein the double clock has a frequency twice that of a reference clock;

divider circuitry coupled to provide an alignment signal corresponding to an inverted double clock divided by two;

a plurality of recovery circuits, each recovery circuit deriving an instance of a first clock and an instance of a second clock from the double clock in accordance with the alignment signal, wherein the first and second clocks associated with each recovery circuit have substantially a 90° phase difference; and

a halt circuit controlling the halt multiplexer control to select the gated generated clock when the alignment signal matches a pre-determined clock level, wherein the halt multiplexer control is clocked by the generated clock.

9. The apparatus of claim 8 wherein the first clock associated with any recovery circuit is substantially synchronized with the first clock associated with any other recovery circuit.

10. The apparatus of claim 8 wherein each recovery circuit comprises:

a first flip-flop receiving the alignment signal, wherein the first flip-flop is clocked by the double clock to provide the first clock; and

a second flip-flop receiving the first clock, wherein the second flip-flop is clocked by an inverted double clock to provide the second clock.

11. The apparatus of claim 10 wherein each of the first and second flip-flops is a D-type flip-flop.

12. The apparatus of claim 8 further comprising a phase locked loop to provide the generated clock, wherein each instance of the first and second clocks has a same frequency as the reference clock, wherein each instance of the first clock is synchronized with the reference clock.

13. The apparatus of claim 8 wherein the divider circuitry further comprises:

an inverter coupled to provide an inverted double clock from the double clock; and

a divider coupled to divide the inverted double clock to provide the alignment signal.

14. The apparatus of claim 8 wherein the clock generator, divider, and recovery circuitry reside on a same integrated circuit die.

15. The apparatus of claim 14 wherein the clock generator, divider and recovery circuitry are formed as a metal oxide semiconductor field effect transistor (MOSFET) integrated circuit.

16. A method of generating a quadrature clock, comprising:

selecting one of a generated clock and a gated generated clock as a double clock in accordance with a halt multiplexer control, wherein the double clock has a frequency twice that of a received reference clock;

generating an alignment signal corresponding to an inverted double clock divided by two;

deriving a plurality of instances of a first clock and an associated second clock from the double clock in accordance with the alignment signal, wherein each first and associated second clock instance have a 90° relative phase difference; and

controlling the halt multiplexer control to select the gated generated clock when the alignment signal matches a pre-determined clock level, wherein the halt multiplexer is clocked by the generated clock.

17. The method of claim 16 wherein deriving each instance of the first clock includes latching the alignment signal in accordance with the double clock to provide the first clock, wherein deriving the each instance of the second clock includes latching the associated first clock in accordance with an inverted double clock to provide the second clock.

18. The method of claim 16 further comprising:
providing differential distribution of the double clock.

19. The method of claim 16 further comprising:
stepping the gated generated clock to step the first and second clock instances through the quadrature clock cycles

20. The method of claim 16 wherein deriving each instance of the first clock further comprises providing the alignment signal to a first latch, wherein the first latch is clocked by the double clock to provide that instance of the first clock.